BACHELOR OF TECHNOLOGY (C.B.C.S.) (2014 COURSE)
B.Tech.Sem - VI Information Technology : WINTER- 2022
SUBJECT : COMPUTER ORGANIZATION & ARCHITECTURE

Day : Tuesday | Time : 10:00 AM-01:00 PM

Date : 29-11-2022 | **W-13425-2022** | Max. Marks : 60

N.B

1) All question are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagrams **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q.1 What is Descriptor table? Explain in brief: GDT, LDT and IDT. **(10)**

OR

Q.1 Explain the function of following pins of 80386 processor **(10)**
i) BS16 ii) $\overline{\text{LOCK}}$ iii) ADS

Q.2 Describe the set associative mapping technique of Cache memory with neat diagram. **(10)**

OR

Q.2 What is Virtual Memory? Explain Page replacement policies in detail. **(10)**

Q.3 Explain and differentiate horizontal and vertical microinstructions. **(10)**

OR

Q.3 Describe Hardwired control unit. Also explain its working with suitable diagram. **(10)**

Q.4 Explain different addressing modes of Pentium processor. **(10)**

OR

Q.4 Describe Cache Organization also explain Cache Coherence. **(10)**

Q.5 Explain RISC architecture with neat diagram. **(10)**

OR

Q.5 Describe following memory modes with suitable diagram: **(10)**
i) UMA ii) NUMA iii) COMA

Q.6 Describe Pipeline Processing and Instruction Pipelining with neat diagram. **(10)**

OR

Q.6 Explain the Berstein's conditions of detecting parallelism. **(10)**

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