BACHELOR OF TECHNOLOGY (C.B.C.S.) (2014 COURSE)
B.Tech.Sem - VI ELECTRONIC : WINTER- 2022
SUBJECT : VLSI DESIGN

Day : Monday | Time : 10:00 AM-01:00 PM

Date : 28-11-2022 | **W-13390-2022** | Max. Marks : 60

N.B.:

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable **CALCULATOR** is allowed.
4) Draw neat and labeled diagrams **WHEREVER** is allowed.
5) Assume suitable data if necessary.

Q.1 Describe VHDL primary constructs with example. **(10)**

OR

Design 4-bit shift register using VHDL. **(10)**

Q.2 Describe the types of FSM with suitable example. List merits and demerits of FSM. **(10)**

OR

Design 1011...sequence detector using VHDL with Meaty machine. **(10)**

Q.3 Draw the architecture of CPLD XC9500. Explore the macro cell and function block. **(10)**

OR

What is the difference between logic implemented in CPLD and FPGA? **(10)**

Q.4 Describe the body effect and MOSFET capacitances. **(10)**

OR

Discuss the MOSFET structure and explain the scaling of MOS circuits. **(10)**

Q.5 Describe CMOS inverter characteristics in detail. **(10)**

OR

Illustrate lambda-based design rules with neat sketches. **(10)**

Q.6 Design two-input NOR gate using CMOS. **(10)**

OR

Design the CMOS logic circuit for the given expression. **(10)**

$$y=\overline{(A+B).(C+D)}$$

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