BACHELOR OF TECHNOLOGY (C.B.C.S.) (2020 COURSE) B.Tech.Sem - III E&C :: SUMMER - 2022

SUBJECT: SWITCHING THEORY & LOGIC DESIGN

S-24593-2022

Time: 02:30 PM-05:30 PM

Max. Marks: 60

Day: Tuesday

Date: 31-05-2022

| N.B. | | |
|------------|--|-------------|
| | 1) All questions are COMPULSORY . | |
| | 2) Figures to the RIGHT indicate FULL marks. | |
| | Use of non-programmable calculator is ALLOWED . | |
| | 4) Assume suitable data WHEREVER necessary. | |
| Q.1 | Convert the following numbers from Decimal to Octal and then to binary. i) 375 ii) 249. | (10) |
| Q.1 | OR | (10) |
| Q.1 | For the logic expression : $Y = AB + AB$, i) obtain the truth table | (10) |
| | i) obtain the truth tableii) name the operation performed | |
| | iii) realise this operation using AND, OR, NOT gates. | |
| | and the second of the second o | |
| Q.2 | Prove the following using De Morgans theorems: | (10) |
| ~ | i) $AB + CD = \overline{AB \cdot CD}$. | ` , |
| | , , , , , , , , , , , , , , , , , , , | |
| | ii) $ (A+B).(C+D) = \overline{\left(\overline{A+B} + \left(\overline{C+D}\right)\right)} . $ | |
| | OR | (10) |
| Q.2 | Minimize the following function and realise using minimum number of gates | (10) |
| | $F = \sum m(0,3,5,6,9,10,12,15) .$ | |
| Q.3 | Design and explain full subtractor circuit using two half subtractors and | (10) |
| • | realisation of full subtractor using NAND gates. | |
| 0.0 | OR | (10) |
| Q.3 | Design a 32:1 multiplexer using two 16:1 multiplexer IC. | (10) |
| Q.4 | Design 3 bit Binary counter. | (10) |
| • | OR | (4.0) |
| Q.4 | Explain the operation of the bi-directional shift register. | (10) |
| 0.5 | Differentiate between | (10) |
| Q.5 | i) RAM and ROM | () |
| | ii) Volatile memory and non-volatile memory. | |
| | OR | (4.0) |
| Q.5 | Explain any 5 characteristics of Digital IC. | (10) |
| Q.6 | Explain in detail VLSI design flow (with reference to EDA tool). | (10) |
| | OR | (10) |
| Q.6 | Write short note on: i) data flow | (10) |
| | i) data flowii) Structural modeling | |
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