

BACHELOR OF TECHNOLOGY (C.B.C.S.) (2021-COURSE)
B. Tech. Sem - I CS& E :SUMMER- 2022
SUBJECT : DIGITAL ELECTRONICS

Day : Thursday
Date : 21-07-2022

S-24021-2022

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N.B.:

- 1) All questions are **COMPUSLORY**.
- 2) Figures to the right indicate **FULL** marks.
- 3) Assume suitable data **WHEREVER** necessary.
- 4) Draw neat labeled diagrams **WHEREVER** necessary.

- Q.1** Perform following operations: **(10)**
- a) Subtract $(42 - 27)$ using 2's complement method.
 - b) Subtract $(13 - 9)$ using 1's complement method.
 - c) Multiply 101.11×111.01
 - d) Divide $(110110) \div (101)$
 - e) Determine Gray code and Excess-3 code for decimal number 12

OR

- Q.1** Explain why NAND and NOR gates are called universal gates. Realize all logic gates using **only NAND** gates. **(10)**
- Q.2** State and explain De-Morgan's theorem Prove that. **(10)**
- a) $A + \overline{A}B = A + B$
 - b) $(A + B)(A + C) = A + BC$

OR

- Q.2** Simplify following SOP expression using K-map and realize using logic gates. **(10)**
 $F(A, B, C, D) = \sum m(1, 3, 4, 5, 6, 9, 13, 15) + d(7, 11)$
- Q.3** State Rules for BCD addition. Design 4 bit BCD adder using two 4 bit Binary adders. **(10)**

OR

- Q.3** Implement following Boolean function using 8:1 Multiplexer. **(10)**
 $F(A, B, C, D) = \sum m(2, 4, 5, 6, 8, 11, 13)$
- Q.4** Distinguish between Synchronous and Asynchronous counters. Design mod 7 counter and draw neat timing diagram. **(10)**

OR

- Q.4** Design 3 bit up-down counter with neat circuit diagram and timing diagram. **(10)**
- Q.5** Compare Moore and Mealy Models with suitable examples write state table and state equation for clocked D flip flop. **(10)**

OR

- Q.5** Describe basic elements ASM chart. Explain Multiplexer controller method with suitable example. **(10)**
- Q.6** Describe PLA with neat block diagram Implement following functions using PLA with 3 inputs, 3 product terms and two outputs. **(10)**
 $F_1(a, b, c) = \sum m(5, 6, 7)$
 $F_2(a, b, c) = \sum m(3, 5, 7)$

OR

- Q.6** Describe different types of PLDs. Design 3 bit Gray to Binary code converter and Implement using PROM. **(10)**

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