BACHELOR OF TECHNOLOGY (C.B.C.S.) (2021-COURSE)

B. Tech. Sem - II CS&E-A&M :SUMMER- 2022

SUBJECT : DIGITAL ELECTRONICS

Day : Wednesday | Time : 10:00 AM-01:00 PM

Date : 3/8/2022 | **S-23932-2022** | Max. Marks : 60

N.B.

1) All questions are **COMPULSORY**.
2) Figure to the right indicate **FULL** marks.
3) Use of non – programmable **CALCULATOR** is allowed.
4) Draw neat and labelled diagram **WHEREVER** necessary.

Q.1 Perform the following operations **(10)**

a) Add 1011 and 1001
b) Subtract 1010 from 1110
c) Multiply 1101 by 110
d) Divide 101101 by 110
e) Subtract 1011 from 1111

OR

Q.1 Why are NAND and NOR gates called universal gates? Derive AND and OR gates using NAND and NOR gates. **(10)**

Q.2 Simplify the following expression using Quine Mc Clusky method and realize it using basic gates. **(10)**
$F(A,B,C,D) = \sum m\ (0,1,3,7,8,9,11,15)$

OR

Q.2 Simplify the following expression using K – map and realize it in universal logic. **(10)**

a) $F(A,B,C,D) = \sum m\ (1,5,6,12,13,14) + d(2,4)$
b) $F(A,B,C) = \pi M\ (0,1,2,3,4,7)$

Q.3 State rules for BCD addition. Design BCD adder using two 4 – bit Binary adders. **(10)**

OR

Q.3 Draw a logic diagram, block diagram and write a k – map simplification from truth table for full Adder. **(10)**

Q.4 Describe working of T – flip flop and SR – flip flop with the help of truth table. **(10)**

OR

Q.4 Differentiate Asynchronous counters and Synchronous counters. Design 2 – bit asynchronous counter using flip flops with the help of timing diagram. **(10)**

Q.5 Design a logic diagram for the serial binary adder. **(10)**

OR

Q.5 Design a logic diagram to detect the sequence 1010. **(10)**

Q.6 Design and Implement 3 – bit Binary to Gray code converter using PLA. **(10)**

OR

Q.6 Describe EEPROM and ROM with its advantages and disadvantages. **(10)**

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