MASTER OF TECHNOLOGY (ELECTRONICS - VLSI) (CBCS - 2015 COURSE)
M. Tech. (Electronics - VLSI) Sem-II :SUMMER- 2022
SUBJECT : ANALOG VLSI DESIGN

Day : Thursday
Date : 28-07-2022

S-14105-2022

Time : 10:00 AM-01:00 PM
Max. Marks : 60

N. B.

1) All Questions are **COMPULSORY**.
2) Both the sections should be written in **SEPARATE** answer books.
3) Figures to the right indicate **FULL** marks.
4) Draw neat labeled diagrams **WHEREVER** necessary.

SECTION-I

Q.1 Using suitable equations and I-V characteristics, derive and explain following: **(10)**
a) R_{ON} b) λ c) g_m

OR

With the help of diagrams and equations, describe MOS modeling.

Q.2 What is MOS switch? How is it useful in Analog Design? Explain using suitable equations and diagrams. **(10)**

OR

What is sub circuit? How is sub circuit used in Analog application? Explain current mirrors.

Q.3 What is cascode amplifier? How is it used in analog design? **(10)**

OR

Find small- signal voltage gain and -3 dB frequency in Hertz for the active load inverter, the current source inverter and push-pull inverter if $W_n = 2\mu m$, $Lp = Ln = 1\mu m$, $W_p = 1\mu m$ and the dc current is 50 μA, Assume $C_{gd} = 4fF$, $C_{bd} = 10$ fF, $C_L = 1pF$ $Kp' = 50\ \mu A/V^2$, $K_{N'} = 110\ \mu A/V^2$ $\lambda n = 0.04$, $\lambda p = 0.05$, $V_{DD} = 5V$.

SECTION-II

Q.4 With reference to OP AMP explain following : **(10)**
a) Compensation of OP-AMP b) PSRR c) Measurement techniques.

OR

Design two stages CMOS OP-AMP for following parameters:
$L = 1\mu m$
$A_V > 3000$ V/V GB=5MHz $V_{DD} = 2.5V$, $V_{SS} = -2.5V$
SR > 10 V/ μs 60° phase margin, V_{out} range = ± 2V ICMR = -1 to 2V, $P_{diss} \leq 2mW$
$Kp' = 50\ \mu A/V^2$, $K_{N'} = 110\ \mu A/V^2$ $V_{TP} = -0.7V$, $V_{TN} = 0.7V$

Q.5 Why is high speed OP-AMP used in Analog design? Describe using suitable diagram. **(10)**

OR

For two-stage, low power CMOS OP AMP calculate gain, Pd, GB and SR if $I_{D5} = 200nA$, $I_{D7} = 500nA$ $L = 1\ \mu m$, values of n are 1.5 and 2.5 for pMOS and nMOS respectively, Cc=5pF, T=27°C, $V_{DD} = 1.5V$, $V_{SS} = -1.5V$, $\lambda n = 0.04$, $\lambda p = 0.05$, kT/q=0.026 mV.

Q.6 How will you design SC Integrators? **(10)**

OR

Explain the principle of switched capacitor circuits. What are the applications of SC circuits?

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