BACHELOR OF TECHNOLOGY (C.B.C.S.) (2014 COURSE)

B.Tech.Sem - VIT::SUMMER - 2022

ursday 6/2022	Time: 10:00 AM-01:00 PM S-13412-2022 Max. Marks: 60	l
N.B.:	 All questions are COMPULSORY. Figures to the right indicate FULL marks. Draw neat labeled diagrams WHEREVER necessary. Assume suitable data if necessary. 	
Q.1	Explain the response of 8086 processor to INTR interrupt.	(1
	OR	
Q.1	Explain the maximum mode configuration of 8086 processor with neat diagram.	(1
Q.2	Explain the following assembler directives: - i) NEAR ii) ASSUME iii) SEGMENT iv) ENDP	(1
	OR	
Q.2	Differentiate between procedure and macro with suitable examples.	(1
Q.3	Explain the internal architecture of 8253 PIT.	(1
	OR	
Q.3	Explain the master – slave mode of 8259 PIC.	(1
Q.4	Explain the loosely coupled configuration of 8086 processor.	(1
	OR	
Q.4	Explain the internal architecture of CISC processor.	(1
Q.5	Explain the on chip data and program memory of 8051 microcontroller.	(1
	OR	
Q.5	Explain the different SFRs of 8051 microcontroller.	(1
Q.6	Explain the following: i) IDE ii) Emulator iii) DSO iv) Logic Analyzer	(1
	OR	

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Explain the interrupt programming of 8051 microcontroller.

Q.6

(10)