Day : Friday   Time : 02:30 PM-05:30 PM

Date : 17-06-2022   **S-13390-2022**   Max. Marks : 60

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N.B.:
1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable **CALCULATOR** is allowed.
4) Draw neat and labeled diagrams **WHEREVER** is allowed.
5) Assume suitable data if necessary.

Q.1 What is the need of attributes in VHDL? Explain any three attributes with **(10)** suitable example.

OR

Write VHDL code for 4-bit binary up/down counter. **(10)**

Q.2 What do you mean by measurability? What are the solutions? Explain any **(10)** one in detail.

OR

Design 110... sequence detector using VHDL with Moore Machine. **(10)**

Q.3 Draw the architecture of FPGA XC4000. Explore logic cell and interconnect **(10)** matrix.

OR

What is the function of 'bus hold logic' and 'hot plugging capability' in **(10)** CPLD? Describe TAP controller.

Q.4 Define MOSFET and describe the fabrication procedure. **(10)**

OR

Discuss the MOSFET current -voltage characteristics. **(10)**

Q.5 Define stick diagram and layout diagram. Design the stick diagram of CMOS **(10)** inverter.

OR

Describe static power and dynamic power dissipation. **(10)**

Q.6 Design two-input NAND gave using CMOS. **(10)**

OR

Design the CMOS logic circuit for the given expression. **(10)**
$$y = \overline{A + B + C}$$

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