BACHELOR OF TECHNOLOGY (C.B.C.S.) (2014 COURSE)
B.Tech.Sem - VIII ELECTRONIC :SUMMER- 2022
SUBJECT : SYSTEM ON CHIP (SOC)

Day : Wednesday | Time : 02:30 PM-05:30 PM
Date : 22-06-2022 | **S-13405-2022** | Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 Describe in brief: An improved design methodology for SOC design. **(10)**

OR

Q. 1 What are the fundamental trends in SOC design? **(10)**

Q. 2 Describe in brief: Six major issues in SOC design. **(10)**

OR

Q. 2 What is Hardware System Structure in SOC design? Also describe hardware trends. **(10)**

Q. 3 Discuss in brief: Accelerating processors for traditional software tasks. **(10)**

OR

Q. 3 Explain in detail: System design with multiple processors. **(10)**

Q. 4 Discuss following terms in brief: **(10)**
Communication Design=Software mode + Hardware Interconnect

OR

Q. 4 Discuss the hardware interconnect mechanism with following: **(10)**

i) Buses
ii) Direct connect ports
iii) Data queues
iv) Time multiplexed processor

Q. 5 What are the three common types of pipeline stalls inside the processor? What are the advantages of pipeline stalls? **(10)**

OR

Q. 5 What are the different methods used for optimizing processor to match hardware? **(10)**

Q. 6 Describe the limitations of general purpose processors and SOC design transition with reference to SOC. **(10)**

OR

Q. 6 Explain following in brief: **(10)**

i) SOC and ROI
ii) The designer's dilemma

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