BACHELOR OF TECHNOLOGY (C.B.C.S.) (2014 COURSE)

B.Tech.Sem - VI E & TC :SUMMER- 2022

SUBJECT : VLSI DESIGN

Day : Friday | Time : 02:30 PM-05:30 PM

Date : 17-06-2022 | **S-13363-2022** | Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labelled diagrams **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 **a)** Which are the layout design rules? Why are they used? **(04)**

b) Draw stick diagram and CMOS based circuit diagram for 2-input NAND. **(06)**

OR

Q. 1 **a)** How will you define VLSI? Draw Y-chart for VLSI Design. **(04)**

b) Using suitable example, discuss design hierarchy, locality, modularity and regularity. **(06)**

Q. 2 What is scaling? Why it is used? Define full voltage and constant voltage scaling. **(10)**

OR

Q. 2 Explain capacitance associated with MOSFET. **(10)**

Q. 3 **a)** How will you define entity? Give suitable example. **(04)**

b) Write VHDL code for 4×1MUX using with-select statement. **(06)**

OR

Q. 3 **a)** What is component? Design 4-bit parallel adder using full adder as a component. Write VHDL code for the same. **(06)**

b) Write VHDL code for 4-bit up-counter. **(04)**

Q. 4 Differentiate Moore and Mealy FSM. Design decimal counter using Moore FSM. Write VHDL code for the same. **(10)**

OR

Q. 4 **a)** Explain FPGA architecture. **(04)**

b) Design state machine diagram for a sequence detector "1001". Write VHDL code for the same. **(06)**

Q. 5 What is the need of low power VLSI design? How power is consumed in CMOS VLSI design? **(10)**

OR

Q. 5 Discuss VTCMOS and MTCMOS w.r.t. low power CMOS design. **(10)**

Q. 6 What is DFT? How it is implemented? **(10)**

OR

Q. 6 **a)** Using suitable example, explain the need of controllability and observability. **(04)**

b) How physical defect is converted in to logical fault? **(06)**

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