BACHELOR OF SCIENCE (COMPUTER SCIENCE) (CBCS - 2018 COURSE) S.Y.B.Sc.(Computer Science) Sem-III :SUMMER- 2022 SUBJECT : DIGITAL SYSTEMS & MICROPROCESSORS

Time: 03:00 PM-06:00 PM Day: Tuesday S-20095-2022 Max. Marks: 60 Date: 12/7/2022 N.B: 1) All questions are **COMPULSORY**. 2) Figures to the right indicate FULL marks. 3) Draw diagrams WHEREVER necessary. 4) Use of **CALCULATOR** and log table is allowed. **Q.1** Attempt **ANY TWO** of the following: (12)Explain the functions of carry flag, parity flag, auxiliary carry flag, zero flag, a) overflow flag and interrupt flag. Explain the concept of associative memory with necessary diagram. **b**) Draw block diagram of 8086 microprocessor and explain execution unit and **c**) bus interface unit. Attempt **ANY TWO** of the following: Q.2 (12)Draw block diagram of Programmable Peripheral Interface and explain the a) function of its different blocks. Explain the working of 2-bit flash ADC with appropriate diagram. b) What is stack? Explain how PUSH and POP instructions are implemented c) in memory stack. Q.3 Attempt **ANY TWO** of the following: (12)State the function of DMA controller. Explain DMA transfer using DMA a) controller with neat diagram. Explain the following addressing modes with one example of each: b) i) Register ii) Direct iii) Immediate With necessary diagram explain R-2R ladder method for digital to analog c) converter. **Q.4** Attempt ANY THREE of the following: (12)State and explain any four rotate instructions. a) Explain any four parameters of analog to digital converter. b) Explain synchronous serial data transfer. c) d) How does the cache memory help to enhance the system performance? Explain. Q.5 Attempt ANY FOUR of the following: (12)State the difference between the following instructions: a) ii) SUB and CMP i)IMUL and MUL iii) JNZ and JZ Explain the role of address bus, data bus and control bus in a computer b) organization. Explain interrupt initiated data transfer. c) State and explain any three assembler directives. d) Draw well-labelled block diagram of UART. e) Explain 3-level memory hierarchy system.

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