S.D.E.

M.C.A. SEM - I : WINTER - 2017

SUBJECT: COMPUTER ORGANISATION AND ARCHITECTURE

Day: **Wednesday** Time: **10.00 A.M. TO 1.00 P.M.**

Date: **13/12/2017** **W-2017-4413** Max. Marks: 80

N.B.:

1) Attempt any **FIVE** questions from Section –I and any **TWO** questions from Section–II.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer books.

SECTION-I

Q.1 What is combinational circuit? Explain full adder in detail. **(10)**

Q.2 Describe binary adder-subtractor with neat diagram in detail. **(10)**

Q.3 Discuss instruction cycle in detail with flowchart. **(10)**

Q.4 What is Interrupt? Explain the types of Interrupts. **(10)**

Q.5 Differentiate between: **(10)**

i) Hardwired control unit and micro-programmed control unit
ii) RISC and CISC

Q.6 Explain DMA working in detail with neat diagram. **(10)**

Q.7 Write short notes on any **TWO** of the following: **(10)**

a) Peripheral devices
b) Logic gates
c) Register transfer

SECTION-II

Q.8 **a)** Solve the following expression using stack: **(08)**

$\left[(3+7)*2\right]*\left[2+3\right]$

b) Solve the following: **(07)**

i) Find 2's complement of: 11100011
ii) 11100010 - 00101010

Q.9 **a)** Show that: **(08)**

i) $(A+B)'(A'+B')=0$

ii) $F+F'=1$

b) Simplify the following Boolean function using K map: **(07)**

$F(A,B,C,D)=\Sigma(0,1,5,8,9,10)$

Q.10 Explain 4 bit bidirectional shift register with parallel load with help of diagram in detail. **(15)**