B. Tech. Sem -VI (E & TC Engg.) (2014 COURSE) (CBCS) :
WINTER - 2017
SUBJECT: VLSI DESIGN

Day : **Wednesday** Time **10.00 AM TO 01.00 PM**
Date : **22/11/2017** **W-2017-2247** Max. Marks: 60

N.B.
1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable calculator is allowed.
4) Assume suitable data if necessary.

Q.1 **a)** Give brief introduction to VLSI. **(04)**

b) What are the basic fabrication steps? Explain in detail. **(06)**

OR

a) Which are the layout design rules? Discuss in brief. **(04)**
b) Draw stick diagram of NOR. **(06)**

Q.2 **a)** Define τ_{PHL} and τ_{PLH} w.r.t. inverter. **(04)**
b) Draw C-V characteristics of MOSFET. **(06)**

OR

a) Define τ_{rise} and τ_{fall} w.r.t. inverter. **(04)**
b) Explain small geometry effects w.r.t. MOSFET. **(06)**

Q.3 **a)** What is the need for using components in VHDL coding? Define component declaration and component instance with an example. **(05)**
b) Write VHDL code for 3:8 decoder. **(05)**

OR

a) Differentiate between signal and variable used in VHDL with an example. **(05)**
b) Write VHDL code for full adder in structural model, using half adder as a component. **(05)**

Q.4 Draw state diagram to detect a sequence "1011" and write VHDL code for the same. **(10)**

OR

a) Draw the general structure of FPGA and explain. **(06)**
b) Write VHDL code for D-flip flop. **(04)**

Q.5 How low power design is implemented through voltage scaling? Discuss in detail. **(10)**

OR

How reduction in capacitance helps in low power design? Explain in detail. **(10)**

Q.6 **a)** Explain the importance of testing. **(04)**
b) Describe scan based techniques. **(06)**

OR

a) Define controllability and observability. **(04)**
b) Explain BIST. **(06)**

* * *