B.Tech. SEM -VI Electronics 2014 Course (CBCS) : WINTER - 2017

SUBJECT: VLSI DESIGN

Day: **Wednesday** Time: **10.00 AM TO 01.00 PM**

Date: **22/11/2017** **W-2017-2213** Max Marks: 60

N.B:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.

Q.1 Describe different types of VHDL modeling with example. **(10)**

OR

Design 4- bit up/down counter using VHDL. **(10)**

Q.2 Define FSM. Discuss various steps used to design a synchronous sequential machine. **(10)**

OR

Design 110 sequence detector using Moore machine. **(10)**

Q.3 Describe the function of "bus hold logic, slew rate control and hot plugging" capability in CPLD. **(10)**

OR

Realize 4- bit BCD to gray code converter using PLA. **(10)**

Q.4 Describe MOSFET capacitances. State the advantages and disadvantages of scaling. **(10)**

OR

Describe body effect, channel- length modulation and subthreshold conduction with neat diagram. **(10)**

Q.5 Describe the steps in making layout of CMOS inverter. **(10)**

OR

Discuss static and dynamic power dissipation in CMOS circuits. **(10)**

Q.6 Design CMOS logic for **(10)**

a) $Y = AB + C$

b) $Z = \overline{ABCD}$

OR

Describe the operation of Transmission gate. Implement 2:1 mux using Transmission gate. **(10)**

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