B.TECH SEM – VII (2007 COURSE) (ELECTRONICS ENGG.) :
WINTER - 2017
SUBJECT : VLSI DESIGN TECHNOLOGY

Day : **Monday**
Date : **22/01/2018**

Time : **02.30 PM TO 05.30 PM**
Max. Marks: 80

W-2017-2582

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in the **SEPARATE** answer books.
3) Draw neat and labeled diagrams **WHEREVER** necessary.
4) Use of non-programmable **CALCULATOR** is allowed.
5) Figures to the right indicate **FULL** marks.
6) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** Write short note on: Configuration. **[05]**

b) Compare Mealy and Moore machine. **[05]**

c) What is the function of slew rate control logic and GRM in FPGA? **[04]**

Q.2 **a)** Describe VHDL primary constructs. **[07]**

b) Write VHDL code for 8:1 mux. **[06]**

Q.3 **a)** Write VHDL code to detect a sequence 1101 using Moore machine. **[06]**

b) What do you mean by metastability? What are the solutions? Describe any one in detail. **[07]**

Q.4 **a)** Draw the architecture of CPLD XC9500. Describe Function block and Fast connect switch matrix. **[07]**

b) Compare FPGA and CPLD. **[06]**

SECTION – II

Q.5 **a)** Write short note on: BiCMOS technology. **[05]**

b) List the advantages and disadvantages of technology scaling. **[04]**

c) Describe global routing. **[05]**

Q.6 **a)** Explain the concept of power distribution and power optimization. **[07]**

b) Write short note on: Off chip connections. **[06]**

Q.7 **a)** Describe CMOS inverter characteristics. **[07]**

b) Write note on: Transmission gate. **[06]**

Q.8 **a)** Design NOR gate using CMOS logic. **[07]**

b) Design CMOS logic for $y = AB + C$. **[06]**

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