B.TECH. SEM -IV (COMPUTER) 2014 COURSE (CBCS) :
WINTER - 2017
SUBJECT: MICROPROCESSORS & MICROCONTROLLERS

Day: **Friday** Time: **02.30 PM TO 05.30 PM**
Date: **24/11/2017** Max. Marks: 60

W-2017-2077

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable calculator is **ALLOWED**.
4) Draw neat and labeled diagram **WHEREVER** necessary.
5) Assume suitable data, if necessary.

Q.1 **a)** Describe architecture of 80386 DX with neat block diagram. **[05]**

b) Explain instruction pipelining in 80386. **[05]**

OR

a) What is memory segmentation? From which address 8086 starts execution after reset. **[05]**

b) Describe the following signals **[05]**
i) $\overline{TEST}$ ii) DT/ $\overline{R}$ iii) MN/ $\overline{MX}$

Q.2 Draw and explain segment selectors and segment descriptors. **[10]**

OR

Describe protected mode register model of 80386. **[10]**

Q.3 Describe the 8259 interrupt controller with neat block diagram. Explain the function of each block. **[10]**

OR

Compare synchronous data transfer with asynchronous data transfer. Draw and explain functional block diagram of 8251 USART. **[10]**

Q.4 List enhanced features of Pentium processor. Explain how memory is organized in Pentium processor. **[10]**

OR

What is Multicore architecture? Explain bus contention in multicore architecture. **[10]**

Q.5 Describe 8051 interrupt structure. Draw the formats of IP and IE registers. **[10]**

OR

Describe TCON and SCON registers of 8051 microcontroller. **[10]**

Q.6 Describe the steps for interfacing stepper motor with 8051 in detail. **[10]**

OR

Explain Timer/ counter programing in 8051 with suitable example. **[10]**

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