B.TECH SEM – VI (2007 COURSE) (COMPUTER ENGG.) :
WINTER - 2017
SUBJECT: MICROPROCESSOR BASED SYSTEMS

Day: **Thursday** Time: **10.00 AM TO 01.00 PM**
Date: **23/11/2017** **W-2017-2507** Max. Marks: 80

N.B.: **1)** **Q. No. 1** and **Q. NO. 5 are COMPULSORY.** Out of the remaining attempt any **TWO** questions from each section.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer book.
4) Assume suitable data if necessary.
5) Draw neat diagrams **WHEREVER** necessary.

SECTION-I

Q.1 **a)** Compare 80386 SX with 80386 DX. **(05)**

b) Draw protected mode programmer's model of 80386. **(05)**

c) What is the use of DPL filed of confirming code segment. **(04)**

Q.2 **a)** Illustrate RESET & HALT activity in 80386. **(07)**

b) Explain Bit scan and test instructions of 80386 with suitable examples. **(06)**

Q.3 **a)** Draw the format of Non-system segment descriptor and explain the functions of its various fields. **(07)**

b) Explain the significance of RPL, CPL and DPL in 80386. **(06)**

Q.4 **a)** Explain the process of leaving and entering the V86 mode. **(07)**

b) Draw the format of Task Gate Descriptor. Explain the significance of TSS descriptor. **(06)**

SECTION-II

Q.5 **a)** Distinguish between interrupts and exceptions. **(05)**

b) What are the design considerations for dual core processors? **(05)**

c) Explain power saving options supported by 8051. **(04)**

Q.6 **a)** Describe 82496 cache controller with neat diagram. **(07)**

b) Explain how 80386 communicate with 80387. State the functions of interfacing signals. **(06)**

Q.7 **a)** Draw and explain Pentium IV architecture. **(07)**

b) Describe SCSI bus controller. **(06)**

Q.8 **a)** Describe mode 2 and mode 3 of 8051 timer. **(07)**

b) Explain interrupt structure of 8051. **(06)**

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