M. TECH.-III (ELECTRONICS V.L.S.I.) (CBCS – 2015 COURSE) : WINTER - 2017

SUBJECT : ELECTIVE – 2 : TESTING AND VERIFICATION OF VLSI DESIGN

Day : **Thursday** Time : **11.00 AM TO 02.00 PM**
Date : **18/01/2018** **W-2017-2882** Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the **SEPARATE** answer books.
4) Assume suitable data, if necessary.

SECTION - I

Q. 1 How will you define verification? How formal verification is performed? Discuss in brief. **(10)**

OR

How verification is related to design reuse? Discuss testing v/s verification. **(10)**

Q. 2 How static tool helps in verification? Explain with suitable example. **(10)**

OR

Differentiate Event v/s Cycle based simulators. **(10)**

Q. 3 What is the purpose of unit level testing? How it is performed? **(10)**

OR

What are the verification strategies? **(10)**

SECTION – II

Q. 4 What are the logical fault models? Explain in brief. **(10)**

OR

Discuss fault detection and fault dominance. **(10)**

Q. 5 Describe in brief: Test generation for sequential circuits. **(10)**

OR

How testable combinational logic circuits are designed? **(10)**

Q. 6 Explain Ad-hoc design with respect to testing. **(10)**

OR

How BIST is implemented? **(10)**

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