M. TECH.-III (ELECTRONICS V.L.S.I.) (CBCS – 2015 COURSE) : WINTER - 2017

SUBJECT: ELECTIVE –I ALGORITHMS FOR VLSI DESIGN AUTOMATION

Day : **Tuesday** Time: **11.00 AM TO 02.00 PM**
Date : **16/01/2018** **W-2017-2880** Max. Marks. : 60

N.B.:

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Answer to the both the sections should be written in **SEPARATE** answer books.
4) Assume suitable data if necessary.

SECTION-I

Q.1 Explain physical design cycle for VLSI design using suitable diagram. **(10)**

OR

Q.1 Define a graph and explain following terms with respect to graph. **(10)**
a) Self loop b) Biparatite graph c) Edge weighted graph d)Hyper graph
e) Directed and undirected graph

Q.2 What is biological evolution? Discuss the Simulated Evolution algorithm based on it. **(10)**

OR

Q.2 What is performance driven partitioning? Explain process of partitioning using this technique. **(10)**

Q.3 Explain various steps of constraint based floor planning algorithm **(10)**

OR

Q.3 How floor planning is done using Integer Programming based approach. **(10)**

SECTION-II

Q.4 Classify global routing algorithms. Explain Lee's algorithm with diagram. **(10)**

OR

Q.4 What is Maze routing? Explain Hadlock's algorithm for routing. How it improves speed? **(10)**

Q.5 Explain Hybrid HVH-VHV router with suitable diagram. **(10)**

OR

Q.5 Explain switch box concept in routing. Explain Greedy router. **(10)**

Q.6 What is over the cell routing? Explain basic OTC routing algorithm with suitable diagram. **(10)**

OR

Q.6 Explain the reasons for minimizing the number of vias in layout. Discuss constrained via minimization. **(10)**

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