B.TECH. SEM -VI ELECTRONICS 2014 COURSE (CBCS) :

WINTER - 2017

SUBJECT: DIGITAL SIGNAL PROCESSING

Day: **Monday** **W-2017-2211** Time: **10.00 AM TO 01.00 PM**

Date: **20/11/2017** Max Marks: 60

N.B:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Use of non- programmable **CALCULATOR** is allowed.
4) Assume suitable data if necessary.

Q.1 **a)** Derive the relationship of DFT with Z- transform. **(05)**

b) Compute 4-point DFT of the sequence x(n)= {0, 1, 2, 3} **(05)**

OR

What are the advantages of fast convolution? **(10)**

A FIR digital filter has the unit impulse response h (n) = {2, 1, 1}. Determine the output sequence in response to the input sequence x(n)= { 3, 0, -2,0, 2,1,0-2, -1, 0, 0}

Q.2 Compute DFT of the sequence $x(n) = n+1$ and $N = 8$. Find $X(k)$ using DIT-FFT algorithm. **(10)**

OR

a) Give the number of complex additions and complex multiplication required for the direct computation of N- point DFT. **(05)**

b) Compute DFT of the sequence $x(n) = \{1, 0, -1, 0\}$ where N = 4 using DIF-FFT algorithm. **(05)**

Q.3 **a)** Discuss in detail cascade form realization of FIR systems. **(05)**

b) Why do FIR filters have inherent linear phase characteristics? **(05)**

OR

The desired frequency response of a low pass filter is **(10)**

$$H_d(e^{j\omega}) = \begin{cases} e^{-j3\omega} & -\frac{3\pi}{4} \le \omega \le \frac{3\pi}{4} \\ 0 & \frac{3\pi}{4} < |\omega| \le \pi \end{cases}$$

Determine $H_d(e^{j\omega})$ for M= 7 using a Hamming window.

Q.4 **a)** What are the drawbacks of direct form realization of IIR systems? **(05)**

b) Discuss the stability of the impulse invariance technique of IIR filter design. **(05)**

OR

Convert the analog filter into digital filter with system function **(10)**

$H(s) = \frac{2}{(s+1)(s+3)}$ with T=0.1 sec

Using Bilinear transformation method.

P.T.O

Q.5 **a)** Describe in detail overflow limit cycles. **(05)**

b) Analyze truncations and round off processes in binary number representation. **(05)**

OR

Explain the effect of coefficient quantization in the computation of FFT. **(10)**

Q.6 **a)** Describe in detail the VLIW architecture. **(05)**

b) What are the advantages of multiple MAC units in DSP processor? **(05)**

OR

List the salient features of TMS320C67XX DSP processor. Explain the data addressing modes supported by TMS 320C67XX. **(10)**

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