M. TECH.-I (ELECTRONICS V.L.S.I.) (CBCS – 2015 COURSE) : WINTER - 2017

SUBJECT: DIGITAL VLSI DESIGN

Day : **Wednesday** Time : **11.00 AM TO 02.00 PM**
Date : **17/01/2018** **W-2017-2781** Max. Marks : **60**

N. B. :

1) All questions are **COMPULSORY**.
2) Both the sections should be written in **SEPARATE** answer books.
3) Figures to the right indicate **FULL** marks.
4) Draw neat labeled diagrams **WHEREVER** necessary.
5) Assume suitable data, if necessary.

SECTION - I

Q.1 Which are the modeling styles used in VHDL? Discuss with suitable example. **(10)**

OR

How package and configuration are declared in VHDL? **(10)**

Q.2 Design 4–bit full adder using structural modeling. Assume 1-bit full adder is available as component. **(10)**

OR

Explain the concept of delta delay and multiple drivers. **(10)**

Q.3 Design 16 x 4 RAM. **(10)**

OR

What is FSM? Design "1001" sequence detector using FSM. **(10)**

SECTION – II

Q.4 How place and route is done? **(10)**

OR

What is RTL synthesis? Discuss with suitable diagram. **(10)**

Q.5 Describe in brief : PLDs. **(10)**

OR

Which are the modes of configuration in PLDs? **(10)**

Q.6 With suitable example discuss how ROM is used to implement any combinational function? **(10)**

OR

How 6 and 7 variable functions are implemented using FPGA? **(10)**

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