

**B.TECH SEM - III (2007 COURSE) (COMPUTER ENGG.) : WINTER
- 2017**

SUBJECT: DIGITAL LOGIC TECHNIQUES

Day: Wednesday
Date: 17/01/2018

Time: 10.00 AM TO 01.00 PM
Max. Marks: 80

W-2017-2364

N.B:

- 1) Attempt **ANY THREE** questions from each section including Q. No. 1 and Q. No. 5 are **COMPULSORY**.
- 2) Answer to the two sections should be written in **SEPARATE** answer books.
- 3) Figures to the right indicate **FULL** marks.
- 4) Assume suitable data, if necessary.
- 5) Draw neat diagram **WHEREVER** necessary.

SECTION-I

- Q.1**
- a) Perform the following binary subtraction by using 2's complement method. (04)
i) $(2)_{10} - (4)_{10}$ ii) $(4)_{10} - (2)_{10}$
 - b) Implement the following using 8:1 Multiplexer. (05)
 $F(P,Q,R,S) = \sum m(0, 1, 3, 4, 8, 9, 15)$
 - c) Implement a 1-bit latch using NAND and NOR gate. (05)
- Q.2**
- a) Reduce the following function using K-map technique and realize it using suitable gates. (07)
 $F(A,B,C,D) = \sum m(0, 1, 4, 8, 9, 10)$
 - b) Perform the following: (06)
i) $(37.31)_{10} = (?)_2$
ii) $(357.45)_{10} = (?)_8$
iii) $(10.1)_2 = (?)_{16}$
- Q.3**
- a) Design a Two-bit TTL NAND gate with the help of neat circuit diagram. (07)
 - b) Design a full subtractor circuit with the help of truth table. (06)
- Q.4**
- a) Design a MOD-5 ripple counter using a suitable flip flop. (07)
 - b) What is race around condition? Discuss method to avoid race around condition in JK flip flop. (06)

SECTION-II

- Q.5**
- a) Write a short note on semiconductor memories. (05)
 - b) Give a brief note on Hazards. (04)
 - c) Write a short note on FPGA. (05)
- Q.6**
- a) Draw and explain MOS static RAM cell. (07)
 - b) Why refresh cycle is necessary in dynamic RAM explain it? (06)
- Q.7**
- a) Design a sequence generator to generate the following sequence using D flip flop. (06)
 $0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 7 \rightarrow 0$
 - b) Draw and explain with proper examples block diagram of Moore and Mealy machines. (07)
- Q.8**
- a) Describe the difference among the programmable logic devices. (07)
 - b) Explain the multiplexer methods of implementing ASM chart. (06)

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