B.Tech Sem – IV (2007 Course) (Electronics) : WINTER - 2017

SUBJECT : DIGITAL ELECTRONICS & LOGIC DESIGN

Day : **Wednesday** Time : **02.30 PM TO 05.30 PM**
Date : **22/11/2017** **W-2017-2417** Max. Marks : 80

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answer to both the sections should be written in the **SEPARATE** answer books.
3) Use of non programmable **CALCULATOR** is allowed.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data wherever necessary.

SECTION – I

Q.1 **a)** Perform the following operation using 2's complement method: **[04]**
i) 48 – 23 **ii)** – 48 – 23
Use 8-bit representation of numbers.
b) State and prove De-Morgan's theorem. **[06]**
c) Write note on PROM. **[04]**

Q.2 **a)** Perform the following conversion: **[06]**
i) $(85.63)_{10} = (?)_2$
ii) $(204)_{10} = (?)_8$
iii) $(0.122)_{10} = (?)_{16}$
b) What is gray code? What is the advantage of gray code? Give one application of gray code. **[07]**

Q.3 **a)** Minimize the expression using Quine McCluskey method. **[09]**
F (A, B, C, D) = $\sum$m (1, 3, 5, 10, 11, 12, 13, 14, 15).
b) Define the term: **[04]**
i) Prime Implicant **ii)** Minterm.

Q.4 **a)** Give a brief note on PLA. **[06]**
b) Describe the operation of two input TTL NAND gate with the help of neat circuit diagram. **[07]**

SECTION – II

Q.5 **a)** Write a brief note on Binary parallel adder. **[05]**
b) State the principle of multiplexer. **[04]**
c) Describe the S – R clocked flip-flop with the help of truth table. **[05]**

Q.6 **a)** Design a full adder circuit using logic gates. **[07]**
b) Describe a 1 – bit comparator using basic logic gates. **[06]**

Q.7 **a)** Implement the following expression using 8:1 multiplexer. **[07]**
Y (A, B, C, D) = $\sum$m (0, 1, 2, 5, 7, 8, 9, 14, 15).
b) What is Encoder? Describe any one type of encoder in detail. **[06]**

Q.8 **a)** What is the shift register? State and explain different modes of shift register. **[07]**
b) Design and implement a MOD – 5 synchronous counter using T – flip-flops. **[06]**