B.Tech. SEM -IV Info. Tech. 2014 Course (CBCS) : WINTER - 2017

SUBJECT : DIGITAL ELECTRONICS & LOGIC DESIGN

Day : **Wednesday** Time : **02.30 PM TO 05.30 PM**

Date : **22/11/2017** **W-2017-2090** Max. Marks : 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Use of non-programmable calculator is allowed.
4) Assume suitable data if necessary.
5) Draw neat and labeled diagrams **WHEREVER** necessary.

Q.1 Describe 1's complement and 2'S complement with example. **(10)**

OR

Explain various characteristics features of Digital ICs.

Q.2 Simplify the following function by using Quine Mc Cluskey method. **(10)**
$F(A,B,C,D) = \sum m(0,5,6,7,9,10,13,14,15)$

OR

Describe Don't case conditions.

Q.3 Design a 3 bit ripple/asynchronous counter using JK flip-flops. **(10)**

OR

Describe 1 Bit Memory Cell.

Q.4 Write the steps to design the sequence detector. **(10)**

OR

What is state table and state diagram? Explain by considering sequential circuit.

Q.5 Describe DRAM with its advantage and disadvantage. **(10)**

OR

Describe RAM with its types.

Q.6 Describe architecture with modeling style. **(10)**

OR

Describe VHDL program format?

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