B.TECH SEM – V (2007 COURSE) (INF. TECH.) : WINTER - 2017

SUBJECT : COMPUTER ORGANIZATION & ARCHITECTURE

Day : **Tuesday**
Date : **16/01/2018**

W-2017-2471

Time : **02.30 PM TO 05.30 PM**
Max. Marks : 80

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in the **SEPARATE** answer books.
3) Draw neat and labeled diagrams **WHEREVER** necessary.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** Explain the concept of content addressable memories. **[05]**

b) Give advantages and disadvantages of interrupt driven I/O. **[05]**

c) Describe various features of 80386 DX processor in brief. **[04]**

Q.2 **a)** Explain the various advanced DRAM organizations. **[07]**

b) With the help of suitable diagram explain the Pentium cache organization. **[06]**

Q.3 **a)** Draw and explain the hardware implementation of Booth's Algorithm. **[07]**

b) Draw and explain direct mapping technique of cache memory. **[06]**

Q.4 **a)** Explain read, write policies in cache memory design. Also explain the terms cache hit and cache miss. **[07]**

b) Explain the protected mode programmer's model of 80386DX processor. **[06]**

SECTION – II

Q.5 **a)** Explain in brief, micro instruction sequencing with neat diagram. **[05]**

b) Write a short note on "cluster computing". **[05]**

c) Differentiate between RISC and CISC architecture. **[04]**

Q.6 **a)** List down the various applications of microprogramming. **[07]**

b) Explain the features of power PC architecture. **[06]**

Q.7 **a)** Draw the multiplier control unit using Delay Element Method. **[07]**

b) Compare hardwired and microprogrammed control units. **[06]**

Q.8 **a)** Explain the loosely coupled microprocessor configuration with neat diagram. **[07]**

b) Discuss the various design issues in machine level parallelism. **[06]**

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