B.TECH. SEM -VI INFO. TECH. 2014 COURSE (CBCS) :
WINTER - 2017
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE

Day: Thursday
Date: 23/11/2017

Time: 10.00 AM TO 01.00 PM
Max. Marks: 60

W-2017-2219

N.B:

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Assume suitable data if **NECESSARY.**

Q.1 Explain the protected mode programmer's model of 80386 processor. **(10)**

OR

Explain the function of following pins of 80386 processor-
i) PEREQ ii) CLK_2 iii) $\overline{ERROR}$

Q.2 Explain the concept of magnetoresistive RAM in detail. **(10)**

OR

What are the various replacement algorithms of cache memory? Explain.

Q.3 Explain the block diagram of microprogrammed control unit in detail. **(10)**

OR

Explain the state-table method of hardwired control unit design with neat diagram.

Q.4 Explain how pipelining is achieved in Pentium processor with neat diagram. **(10)**

OR

Explain the internal architecture of Pentium processor with neat figure.

Q.5 Explain the SPARC architecture with neat diagram. **(10)**

OR

Explain the concept of multicore architecture in detail.

Q.6 Explain the Handler's classification of parallel processing with suitable example. **(10)**

OR

How the performance of a pipeline is measured? Explain in detail.