B.TECH SEM – V (2007 COURSE) (COMPUTER ENGG.) : WINTER - 2017

SUBJECT : COMPUTER ORGANIZATION

Day : **Thursday**
Date : **18/01/2018**

Time : **02.30 PM TO 05.30 PM**
Max. Marks : 80

W-2017-2457

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in the **SEPARATE** answer books.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** Draw and explain IEEE floating point formats. **[05]**

b) Describe PDP – 11 system with neat block diagram. **[05]**

c) Draw EFLAG register of 80386. **[04]**

Q.2 **a)** What are interconnection structures? Explain various types of bus interconnections. **[07]**

b) Explain instruction cycle with the help of state diagram. **[06]**

Q.3 **a)** Draw hardware implementation for multiplying signed numbers using Booth's algorithm. **[07]**

b) Perform following division using non-restoring division algorithm Dividend = 1010 Divisor = 0011. **[06]**

Q.4 **a)** Explain how instruction pipelining is achieved in 80386. **[06]**

b) Describe addressing modes of 80386 with suitable examples. **[07]**

SECTION – II

Q.5 **a)** Compare horizontal and vertical microinstruction. **[05]**

b) Explain the characteristics of EDO RAM. **[05]**

c) Explain how 80386 communicate with 80387. **[04]**

Q.6 **a)** Describe microprogrammed control unit with neat block diagram. **[07]**

b) Describe structure of 4-bit ALU 2901 with neat diagram. **[06]**

Q.7 **a)** If main memory is of 64K and Cache is of 2K with each block consists of 128 words. Explain how memory address can be mapped in set associative Cache **[07]**

b) List and explain characteristics of memory system. **[06]**

Q.8 **a)** What is the problem of Bus contention? How it can be resolved? **[07]**

b) Compare closely coupled and loosely coupled configurations. **[06]**

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