B.SC. (I. T.) SEM. - I (CBCS - 2015 COURSE) : WINTER - 2017

SUBJECT: DIGITAL ELECTRONICS AND COMMUNICATIONS

Day: **Tuesday** Time: **10.00 A.M. TO 01.00 P.M.**

Date: **19/12/2017** Max. Marks: 60

W-2017-0844

N.B.:

1) Attempt any **SIX** questions.
2) Figures to the right indicate **FULL** marks.
3) Draw neat labeled diagrams **WHEREVER** necessary.
4) Be brief.

Q.1 Draw the diagram of a half- adder. Using half-adders, show the implementation of a full–adder, capable of adding two 4-bit numbers. Use a block representation for a half-adder, when showing implementation for the full-adder. **[10]**

Q.2 Design a combinational circuit with 3 inputs x, y, z and 3 outputs a, b, c when the binary input is 0,1,2 or 3, the binary output is one greater than the input; When the binary input is 4, 5, 6 or 7 the binary output is one less than the input. **[10]**

Q.3 What do you understand by "tri-state" logic? Clearly explain the application of tri–stated devices in digital circuits. **[10]**

Q.4 Draw and explain block diagram of a typical Read / Write memory chip, clearly showing all the inputs, outputs and control lines. **[10]**

Q.5 State Nyquist sampling theorem. Explain the steps involved in converting an analog signal into a digital signal. **[10]**

Q.6 Explain BPSK. Can a PSK scheme be used for modulating analog signals? Briefly explain. **[10]**

Q.7 Compare the merits and demerits of satellite communication and optical fiber communication. **[10]**

Q.8 Draw the diagram of a JK flip flop with PRESET and CLEAR inputs using NAND gates. Show the state table and briefly explain its operation. **[10]**

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