B.Tech. SEM -VI Electronics 2014 Course (CBCS) : WINTER - 2018

SUBJECT : VLSI DESIGN

Day : Thursday
Date : 15/11/2018

W-2018-2480

Time : 10.00 AM TO 01.00 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat diagrams **WHEREVER** necessary.

Q.1 Describe VHDL primary contructs with example. **(10)**

OR

Q.1 Design 4- bit up / down counter using VHDL. **(10)**

Q.2 **a)** Compare Mealy and Moore FSM. **(05)**
b) Describe design steps for synchronous sequential machine. **(05)**

OR

Q.2 Design 1011 sequence detector by mealy machine. **(10)**

Q.3 Realize the following function using PLA **(10)**

$$f_1(A,B,C)=\sum m(1,4,6)$$
$$f_2(A,B,C)=\sum m(0,2,3,7)$$
$$f_3(A,B,C)=\sum m(0,1,4,6)$$

OR

Q.3 Draw the architecture of CPLD XC9500. Describe the function of function block and IOB. **(10)**

Q.4 Describe second order effects considered in MOS analysis. **(10)**

OR

Q.4 Write short note on:

a) MOS capacitances **(05)**
b) MOS small signal model **(05)**

Q.5 Describe static and dynamic power dissipation in detail. **(10)**

OR

Q.5 **a)** Discuss CMOS parasitics. **(05)**
b) Write note on : BiCMOS technology **(05)**

Q.6 Implement half adder using CMOS. **(10)**

OR

Q.6 Implement two input NOR and OR gate using CMOS. **(10)**

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