B.Tech Sem – VII (2007 Course) (Electronics Engg.) : WINTER - 2018

SUBJECT : VLSI DESIGN TECHNOLOGY

Day : Monday
Date : 03/12/2018

W-2018-2925

Time : 02.30 PM TO 05.30 PM
Max. Marks : 80

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in **SEPARATE** answer book.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** Compare data flow, behavioral and structural modeling. **[05]**

b) Explain timing consideration in sequential machine. **[04]**

c) What is the need of 'fast connect switch matrix and bus hold logic' in FPGA/CPLD? **[05]**

Q.2 **a)** Describe VHDL primary constructs. **[07]**

b) Write VHDL code for 4-bit up/down counter. **[06]**

Q.3 **a)** Define FSM. Describe various steps used to design a synchronous sequential machine. **[06]**

b) Write VHDL code for 1011 sequence detector using mealy machine. **[07]**

Q.4 **a)** What is the difference between logic implemented in CPLD and logic implemented in FPGA? **[06]**

b) Draw the architecture of FPGA. Explore the interconnect matrix and logic cell. **[07]**

SECTION – II

Q.5 **a)** Write note on: power distribution. **[05]**

b) Describe Pseudo-nmos logic. **[05]**

c) What are Lambda rules for CMOS layout? **[04]**

Q.6 **a)** Explain on chip I/O architecture in detail. **[06]**

b) What is clock distribution? Describe the types of clock distribution. **[07]**

Q.7 **a)** Describe static and dynamic power dissipation in CMOS. **[07]**

b) Describe body effect. **[06]**

Q.8 **a)** Design two input OR gate using CMOS. **[07]**

b) Describe two phase clocking method. **[06]**

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