B.Tech Sem – VI (2007 Course) (Computer Engg.) : WINTER - 2018

SUBJECT: MICROPROCESSOR BASED SYSTEMS

Day: Friday | **W-2018-2850** | Time: 10.00 AM TO 01.00 PM

Date: 16/11/2018 | Max. Marks: 80

N.B.:

1) **Q. No. 1** and **Q. No. 5** are **COMPULSORY**. Out of the remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer books.
4) Use of non programmable **calculator** is **ALLOWED**.
5) Draw neat and labeled diagrams **WHEREVER** necessary.
6) Assume suitable data, if necessary.

SECTION – I

Q.1	**a)**	Describe dynamic bus sizing in 80386.	**(04)**
	b)	Compare real mode and protected mode.	**(06)**
	c)	Explain any two addressing mode of 80386 with example.	**(04)**
Q.2	**a)**	Explain the difference between 80386SX and DX.	**(06)**
	b)	Explain EFLAG register of 80386 in detail.	**(07)**
Q.3	**a)**	Explain protected mode programmer is model of with neat diagram.	**(07)**
	b)	Give the data types of 80386.	**(06)**
Q.4	**a)**	Define the privilege level. Explain each privilege level in detail.	**(07)**
	b)	Explain the difference between TSS descriptor and task gate descriptor.	**(06)**

SECTION – II

Q.5	**a)**	Explain the significance of Interrupt vector table (IVT).	**(05)**
	b)	Describe PCI bus architecture.	**(04)**
	c)	Explain power saving options supported by 8051.	**(05)**
Q.6	**a)**	Explain the difference between interrupt, fault, trap and abort.	**(06)**
	b)	Draw and explain the block diagram of 82496 cache controller.	**(07)**
Q.7	**a)**	Explain PC Add-on card design considerations.	**(07)**
	b)	Define multicore architecture compare core to duo and dual core processors.	**(06)**
Q.8	**a)**	Explain the interrupt structure in 8051 micro-controller.	**(07)**
	b)	Give specification of Laptops - Sony, Dell, Lenova.	**(06)**

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