M. Tech.-III (Electronics V.L.S.I.) (CBCS – 2015 Course) :
WINTER - 2018
SUBJECT: EIECTIVE- II b) TESTING AND VERIFICACTION OF VLSI DESIGN

Day: Thursday
Date: 06/12/2018

W-2018-3214

Time: 11.00 AM TO 02.00 PM
Max Marks: 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to right **INDICATE** maximum marks.
3) Assume suitable data **WHENEVER** necessary.

SECTION-I

Q.1 What is Functional Verification? Which are the Functional Verification approaches? Explain in brief. **(10)**

OR

Q.1 How will you define Verification? What is the importance of Verification? Differentiate Testing and Verification. **(10)**

Q.2 How Waveform Viewers help in Verification process? Explain using diagrams. **(10)**

OR

Q.2 What is Code Coverage? Describe with examples. **(10)**

Q.3 What is the role of Verification Plan? How it is defined? **(10)**

OR

Q.3 What are the levels of Verification? Explain any one. **(10)**

SECTION-II

Q.4 How will you define Testing? How faults are modeled? **(10)**

OR

Q.4 Which are the types of faults occurred in digital circuits? Explain any four in detail. **(10)**

Q.5 How Testable Combinational logic circuits are designed? **(10)**

OR

Q.5 Describe Test Generation for Sequential circuit. **(10)**

Q.6 What is DFT? How Ad-hoc designs are implemented? **(10)**

OR

Q.6 Why Scan based Designs are used? Discuss in detail. **(10)**

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