B. Tech. Sem - III (Computer Engg.) 2014 COURSE) (CBCS) :
WINTER - 2018

SUBJECT: DIGITAL TECHNIQUES AND LOGIC DESIGN

Day : Wednesday
Date : 28/11/2018

W-2018-2293

Time : 10.00 AM TO 01.00 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 Simplify the following expressions and implement using logic gates: **(10)**

i) $Y = ABC + B\bar{C}D + \bar{A}BC$

ii) $Y = (AB + BC)C$

OR

Describe with neat circuit diagram why NAND and NOR gates are called universal gates. **(10)**

Q. 2 Design 16: 1 Multiplexer using 4: 1 Multiplexers. Write truth table and list applications of Multiplexer. **(10)**

OR

Design and implement Binary to BCD code converter. **(10)**

Q. 3 Describe different modes of Universal shift register with neat diagram. **(10)**

OR

Design and implement 3 bit up down binary ripple counter. Draw timing diagram. **(10)**

Q. 4 Draw and explain EPROM structure. How EPROMs are programmed? **(10)**

OR

Describe structure of DRAM cell and justify the need of refreshing DRAM. **(10)**

Q. 5 Distinguish between CPLD and FPGA structures with respect to following: **(10)**

i) Block diagram
ii) Density of devices
iii) Programmability and volatility

OR

Draw ASM chart and state diagram for a two bit up counter with output Q_1 and Q_0 and enable signal E. Design the circuit using JK flip flops. **(10)**

Q. 6 Describe the fundamental units of VHDL code with suitable examples. **(10)**

OR

Describe different modeling styles of VHDL with suitable examples. **(10)**

* * * * *