

Day: Tuesday
Date: 13/11/2018

W-2018-2478

Time: 10.00 AM TO 01.00 PM
Max. Marks: 60

N.B.:

- 1) All questions are **COMPULSORY**.
- 2) Figures to the right indicate **FULL** marks.
- 3) Draw neat diagrams **WHEREVER** necessary.

Q.1 Determine 8-point DFT of the sequence using direct computation method. (10)
 $x(n)=\{1,1,1,1,1,1,0,0\}$

OR

Q.1 a) State and explain following properties of DFT (04)
i) Linearity ii) Multiplication

b) Compute Circular convolution of the following sequences using concentric circle method. (06)

$$x(n)=\{0,1,2,3\} \quad , \quad h(n)=\{2,1,1,2\}$$

Q.2 Determine DFT of the following sequence using radix-2 DIF-FFT algorithm. (10)
 $x(n)=\{1,1,1,1,1,0,0,1\}$

OR

Q.2 a) What is twiddle factor? State and explain its properties. (06)

b) Explain computational efficiency of Radix-2 FFT algorithm. (04)

Q.3 Determine $h_d(n)$ and $H(e^{j\omega})$ of the digital filter with the desired frequency response (10)

$$H_d(e^{j\omega}) = 0 \quad ; \quad -\frac{\pi}{4} \leq \omega \leq \frac{\pi}{4}$$

$$e^{-2j\omega} \quad ; \quad \frac{\pi}{4} \leq |\omega| \leq \pi$$

$$w(n) = 1 \quad ; \quad 0 \leq n \leq 5$$

$$= 0 \quad ; \quad \text{otherwise}$$

OR

Q.3 a) A digital filter has the following impulse response $h(n)=\{-3,2,1,-2,3\}$. If it is linear phase, Justify. (05)

b) What are the desirable features of FIR filter? (05)

Q.4 Derive mapping formula for Bilinear transformation method for IIR filter. What is warping effect? (10)

OR

Q.4 a) What are advantages and disadvantages of bilinear transformation method? (05)

b) What is mapping procedure between S-plane and Z-plane? (05)

P.T.O

- Q.5 a)** Explain the errors which arise due to the quantization process. **(05)**
b) What is coefficient quantization error? **(05)**

OR

- Q.5 a)** Why rounding is preferred error to truncation in realizing digital filter? **(05)**
b) What do you mean by overflow oscillation? **(05)**

- Q.6 a)** What are the differences between fixed type and floating type processors? **(05)**
b) Describe the various addressing modes used in TMS 320 C6XX processor. **(05)**

OR

- Q.6** Draw and explain architectural block diagram of TMS320C6XX processor. **(10)**

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