M. Tech.-I (Electronics V.L.S.I.) (CBCS – 2015 Course) : WINTER 2018

SUBJECT : DIGITAL VLSI DESIGN

Day : Wednesday
Date : 05/12/2018

W-2018-3113

Time : 11.00 AM TO 02.00 PM
Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagrams **WHEREVER** necessary.
4) Assume suitable data if necessary.

SECTION - I

Q.1 Explain the following terms with respect to processing of VHDL code: **[10]**
a) Analysis **b)** Elaboration **c)** Execution

OR

Explain the building blocks of VHDL code.

Q.2 Explain the use of generics with a suitable example. **[10]**

OR

Write VHDL code for 3:8 decoder.

Q.3 Differentiate between Mealy and Moore machine with neat block diagrams. **[10]**

OR

Write VHDL code to detect "10011001" sequence.

SECTION - II

Q.4 Explain the terms with reference to FPGA: **[10]**
a) Floor planning b) Place and Route

OR

Explain the typical design flow for CPLD based digital design.

Q.5 What is a "Macro Cell" in CPLD? Explain with a neat diagram. **[10]**

OR

Explain the terms with reference to FPGA : a) Logic Capacity b) Logic Density c) Speed- performance d) Logic Block e) Interconnects

Q.6 Realize the following logic function using AND-OR planes: **[10]**
Y=AB+CDE

OR

Explain the fusible link and anti-fuse with respect to programming technology.

* * * *