B.Tech Sem - III (2007 Course) (Computer Engg.) : WINTER - 2018
SUBJECT: DIGITAL LOGIC TECHNIQUES

Day : Wednesday
Date : 28/11/2018

W-2018-2707

Time : 10.00 AM TO 01.00 PM
Max. Marks: 80

N. B. :

1) **Q. No.1** and **Q. No. 5** are **COMPULSORY**. Out of remaining attempt **Any TWO** questions from each section.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the **SEPARATE** answer book.
4) Neat diagrams must be drawn **WHEREVER** necessary.

SECTION-I

Q.1 **a)** Carry out following conversions. **(06)**
i) $(A92)_{16} = (\quad)_8$
ii) $(61.3)_{10} = (\quad)_2$
iii) $(574)_8 = (\quad)_{10}$

b) State the features of CMOS Logic. **(04)**

c) What is function of Shift Register? State its applications. **(04)**

Q.2 **a)** Simplify following function using K map and implement using logic gates. **(07)**
$Y = \sum m\,(1,3,5,9,11,13)$.

b) State Boolean laws and prove the following Boolean Expression **(06)**
$(A+B)\,(A+C) = A+BC$.

Q.3 **a)** Design parity generator using basic gates to produce digital word with odd parity. **(07)**

b) Describe the operation of TTL tristate inverter with the help of neat circuit diagram. **(06)**

Q.4 **a)** How will you convert JK Flip Flop into T Flip Flop and D Flip Flop? Describe applications of T Flip Flop and D Flip Flop in sequential circuit. **(07)**

b) What is MOD counter? Design Mod -7 Asynchronous counter using JK flip flop. **(06)**

SECTION-II

Q.5 **a)** Classify different types of ROM and state their applications. **(06)**

b) Describe the general form of Mealy circuit with example **(04)**

c) Distinguish between CPLD & FPGA. **(04)**

Q.6 **a)** Describe the different types of semiconductor memories. **(07)**

b) Describe the structure and programming of EPROM with neat diagram. **(06)**

Q.7 **a)** Design a sequence generator to generate the sequence 1-3-5-7-6. **(07)**

b) Design 3-bit Synchronous UP counter. **(06)**

Q.8 **a)** Compare Data flow, Structural and Behavioural modeling in VHDL. **(07)**

b) Draw ASM chart for sequential circuit with control input E and counts down from 3 to 0. **(06)**

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