

Day: Friday
Date: 16/11/2018

W-2018-2368

Time: 02.30 PM TO 05.30 PM
Max Marks: 60

N.B.:

- 1) All questions are **COMPULSORY**.
 - 2) Figures to the right indicate **FULL** marks.
 - 3) Draw neat labeled diagrams **WHENEVER** necessary.
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Q.1 Describe the following simplification techniques with the help of example. **(10)**

- i)** Simplification using Boolean Algebra laws
- ii)** Simplification using Karnaugh map(k-map)
- iii)** Simplification using Quine Mc-cluskey method.

OR

Q.1 State and describe the following binary codes: **(10)**

- i)** BCD code **ii)** Gray code **iii)** Excess-3 code
- iv)** ASCII **v)** Error detecting and correcting codes

Q.2 Design a 4-bit BCD to Excess-3 code converter and implement using logic gates. **(10)**

OR

Q.2 **a)** Design a 1-bit comparator using basic gates. **(06)**
b) Write a short note on Look Ahead carry Generator. **(04)**

Q.3 **a)** With the help of neat diagram describe the working of 2-input TTL NAND gate. **(06)**

b) Briefly describe the Tristate TTL logic. **(04)**

OR

Q.3 Define the following parameters of digital IC families and give their typical values for TTL and CMOS families. **(10)**

- i)** Propagation delay **ii)** Noise margin
- iii)** Fan out **iv)** Figure of Merit

Q.4 **a)** State and describe the triggering methods used for Flip Flops. **(06)**

b) What is the function of Preset and Clear inputs in Flip Flop. **(04)**

OR

Q.4 For the clocked D Flip Flop write the state table draw the state diagram and write the state equation. **(10)**

Q.5 Draw the schematic diagram of a 4-bit asynchronous up-down counter and describe with the help of waveforms. **(10)**

OR

Q.5 With a neat diagram describe the operation of 4-bit SISO (Serial-in-Serial-out) left shift register. Draw the timing diagram and give its truth table. **(10)**

Q.6 Describe the concept of PLA and PAL with the help of a block diagram. **(10)**

OR

Q.6 Differentiate between the following: **(10)**

- i)** Static and Dynamic RAM
- ii)** RAM and ROM
- iii)** EPROM and EEPROM