B.Tech. SEM -IV Info. Tech. 2014 Course (CBCS) : WINTER - 2018

SUBJECT: DIGITAL ELECTRONICS AND LOGIC DESIGN

Day: Thursday
Date: 15/11/2018

W-2018-2354

Time: 02.30 PM TO 05.30 PM
Max Marks: 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw diagrams **WHEREVER** necessary.

Q.1	Explain tri-state logic with suitable example.	**(10)**
	OR	
Q.1	Discuss decimal to octal and decimal to binary, number conversion with suitable example.	**(10)**
Q.2	Explain don't care conditions with suitable example.	**(10)**
	OR	
Q.2	Simplify using k-map $F(a,b,c,d)= \sum (0,1,2,3,5,7,8,9,11,14)$	**(10)**
Q.3	Discuss excitation table for flip flops.	**(10)**
	OR	
Q.3	Explain 1- bit memory cell in detail.	**(10)**
Q.4	Explain mealy machine representation.	**(10)**
	OR	
Q.4	Explain state diagram and state table with suitable example.	**(10)**
Q.5	Explain synchronous SRAM with its advantages and disadvantages.	**(10)**
	OR	
Q.5	Describe expanding memory size with suitable example.	**(10)**
Q.6	Describe design example using VHDL for basic combinational circuits.	**(10)**
	OR	
Q.6	Describe VHDL architecture with suitable example.	**(10)**

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