B.Sc. (I. T.) Sem. - I (2011 Course) : WINTER - 2018

SUBJECT: COMPUTER ARCHITECTURE

Day: Monday
Date: 26/11/2018

W-2018-1094

Time: 02.30 pm to 05.30 pm
Max. Marks: 80

N.B.:

1) Attempt Any **FIVE** full questions
2) Figures to the right indicate **FULL** marks.
3) Draw neat, labeled diagrams **WHEREVER** necessary.

Q.1 **a)** Simplify the following expressions using Boolean theorems and identities:- **[06]**

i) $F(x, y, z) = x'z + x'y + xy'z + yz$

ii) $F(A, B) = AB + A'B$

b) Explain, using a Truth Table, the functioning of a JK flip- flop. How is a JK flip flop used to store data? **[10]**

Q.2 An even parity generator is a device that adds an extra bit to data to make the total number of 1's in the data even. Write the Truth Table for a 3-bit even parity generator and show its construction using logic gates. Use K- map to simplify the expression. **[16]**

Q.3 **a)** Show, diagrammatically the construction of a Half-Adder. Explain how half-adders can be used to construct a full-adder. **[10]**

b) Convert the following OCTAL numbers into binary, hexadecimal and decimal **[06]**

i) 651 ; ii) 6637

Q.4 **a)** Clearly explain the difference between SRAM and DRAM Highlight their uses. **[08]**

b) What do you understand by "Memory Hierarchy?" How is memory organized hierarchically? **[08]**

Q.5 Explain what is I/O interfacing and why it is required. Compare the isolated and memory-mapped methods of I/O interfacing. **[16]**

Q.6 Write short notes on **ANY TWO** of the following: **[16]**

a) Set associative mapping of cache

b) Virtual memory

c) Edge-triggered Flip Flop

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