B.TECH. SEM -VI ELECTRONICS 2014 COURSE (CBCS) :
SUMMER - 2018
SUBJECT: VLSI DESIGN

Day: **Wednesday** | **S-2018-2425** | Time: **02.30 PM TO 05.30 PM**
Date: **06/06/2018** | Max Marks: 60

N.B:
1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.

Q.1 Describe VLSI design flow in detail. **(10)**

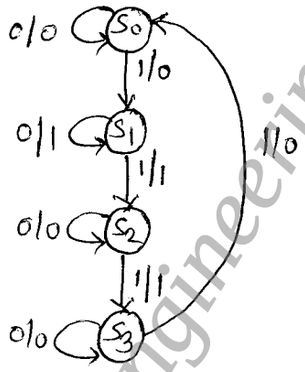
OR

Design 4- bit universal shift register. **(10)**

Q.2 **a)** Write short note on: state diagram. **(05)**
b) Compare Moore and Mealy machine. **(05)**

OR

Design sequential circuit described by following state diagram using VHDL. **(10)**



Q.3 Draw FPGA architecture with neat diagram and describe input -output block and LUTs. **(10)**

OR

Draw the architecture of XC9500 and describe macrocell and fast connect switch matrix. **(10)**

Q.4 Describe MOS source follower and derive expression for A_v and R_{out}. **(10)**

OR

Describe common source amplifier and derive expression for small signal voltage gain. **(10)**

Q.5 Describe regularity, modularity and locality. **(10)**

OR

Describe layout design rules. **(10)**

Q.6 Design CMOR NOR gate and NAND gate. **(10)**

OR

a) Draw CMOS logic schematic for **(05)**
$Y = AB + \overline{A}\,\overline{B}$

b) Calculate area on chip of three-input NAND gate for 120 nm process. **(05)**

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