B.TECH SEM – VII (2007 COURSE) (ELECTRONICS ENGG.) : SUMMER - 2018

SUBJECT : VLSI DESIGN TECHNOLOGY

Day : **Friday** | Time : **02.30 PM TO 05.30 PM**
Date : **25/05/2018** | **S-2018-2787** | Max. Marks : 80

N.B.:

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of the remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in **SEPARATE** answer book.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Figures to the right indicate **FULL** marks.
5) Assume suitable data if necessary.

SECTION – I

Q.1 **a)** Differentiate between function and procedure. **[05]**

b) Differentiate between synchronous and asynchronous machines. **[04]**

c) What is the function of 'bus hold logic and slew rate control' in FPGA/CPLD? **[05]**

Q.2 **a)** What is the need of configuration? Explain configuration binding with example. **[06]**

b) Write VHDL code for BCD to 7-segment decoder for single digit LED display. **[07]**

Q.3 **a)** Explain Mealy and Moore machine. **[06]**

b) Design 110 sequence detector using Moore Machine. **[07]**

Q.4 **a)** Compare CPLD and FPGA. **[06]**

b) Describe PLA with neat diagram. Realize half adder using PLA. **[07]**

SECTION – II

Q.5 **a)** Write note on: Design Validation. **[05]**

b) Describe transmission gate logic. **[05]**

c) Write note on: Dynamic CMOS logic. **[04]**

Q.6 **a)** Describe global routing and switch box routing. **[06]**

b) Write note on: I/O architecture. **[07]**

Q.7 **a)** Describe the steps to create physical layout of CMOS inverter. **[07]**

b) Design 2:1 mux using transmission gate. **[06]**

Q.8 **a)** Design the following function using CMOS logic: **[07]**
$y = \overline{a.(b+c).(d+e)}$

b) Describe regularity with example. **[06]**

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