

**M. TECH.-III (ELECTRONICS V.L.S.I.) (CBCS – 2015
COURSE) : SUMMER - 2018**
SUBJECT: ELECTIVE-I: PROGRAMMABLE SYSTEM ON CHIP

Day: Tuesday S-2018-3072 Time: 11.00 AM TO 02.00 PM
Date: 29/05/2018 Max. Marks: 60

N.B:

- 1) All questions are **COMPULSORY**.
 - 2) Figures to the right indicate **FULL** marks.
 - 3) Answers to both the sections should be written in the **SEPARATE** answer book.
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SECTION-I

Q.1 Explain and compare the features of PSoC1, PSoC2 and PSoC3 Families. (10)

OR

What do you mean by programmable routing and interconnections used in PSoC? (10)

Q.2 With neat schematic, explain the architecture of PSoC5. Compare PSoC3 and PSoC5. (10)

OR

Explain the architecture of following subsystems used in PSoC. (10)
i) CPU Subsystem, ii) I/O Interface

Q.3 Write a short note on "PSoC Designer Suit". (10)

OR

Explain with neat diagram Memory Management in PSoC. (10)

SECTION-II

Q.4 What are the hardware and software subsystems used in mixed signal architecture of PSoC. Explain each in detail. (10)

OR

Explain in detail PSoC Express. Design any mixed signal embedded system using PSoC express. (10)

Q.5 Explain the working of Universal Digital Block and Digital System Interconnect of PSoC with the help of neat diagram. (10)

OR

What are the differences between op-amp and programmable gain amplifiers? What is the use of switched capacitor in amplifiers? (10)

Q.6 Design and implement Data Acquisition and Control System using PSoC. (10)

OR

Explain in detail how SPI and UART is used for communication between two tasks. (10)

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