B.TECH SEM – VI (2007 COURSE) (COMPUTER ENGG.) :
SUMMER - 2018
SUBJECT: MICROPROCESSOR BASED SYSTEMS

Day: **Friday** Time: **02.30 PM TO 05.30 PM**
Date: **08/06/2018** **S-2018-2712** Max. Marks: 80

N.B.:

1) **Q. No. 1** and **Q. No. 5** are **COMPULSORY**. Out of the remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer books.
4) Use of non programmable **calculator** is **ALLOWED**.
5) Draw neat and labeled diagrams **WHEREVER** necessary.
6) Assume suitable data, if necessary.

SECTION - I

Q.1 **a)** Explain the difference between 80386SX and DX. **(04)**

b) Give programming model of 80386SX with figure. **(06)**

c) Explain the following pins 1) HOLD 2) HLDA 3) RESET 4) ERROR **(04)**

Q.2 **a)** Draw and explain functional block diagram of 80386 processor. **(07)**

b) Explain segment and segmentation in detail. **(06)**

Q.3 **a)** Explain protected mode address translation in detail with diagram. **(07)**

b) Explain how to switch from real mode to VM86. **(06)**

Q.4 **a)** Explain linear to physical address translation. **(07)**

b) Explain task switching and task gate. **(06)**

SECTION – II

Q.5 **a)** Explain 82496 cache controllers. **(05)**

b) Justify difference between single core and multicore. **(05)**

c) Explain SFR of 8051. **(04)**

Q.6 **a)** Draw and explain block diagram of 82491 cache SRAM. **(07)**

b) Give cache organization for Pentium family. **(06)**

Q.7 **a)** Draw and explain Pentium-IV architecture. **(07)**

b) Explain SCSI bus controller in detail. **(06)**

Q.8 **a)** Explain the difference between microprocessor and microcontroller. **(06)**

b) Give features of MCS - 31/51 and also data type of 8051. **(07)**

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