B.TECH SEM – IV (2007 COURSE) (ELECTRICAL ENGG.) :
SUMMER - 2018
SUBJECT: LINEAR & DIGITAL INTEGRATED CIRCUITS

Day: **Saturday** Time: **10.00 AM TO 01.00 PM**
Date: **02/06/2018** **S-2018-2615** Max Marks: 80

N.B:

1) Q. No. **1** and Q. No. **5** are **COMPULSORY**. Out of remaining attempt **ANY TWO** questions from Section – **I** and Section – **II**.
2) Figures to the right indicate **FULL** marks.
3) Answer to both the sections should be written in **SEPARATE** answer books.
4) Draw neat and labeled diagrams **WHENEVER** necessary.
5) Assume suitable data, if necessary.

SECTION – I

Q.1 **a)** Define i)input offset current ii) Input offset voltage .State its values for operational amplifier **(04)**

b) Draw circuit diagram of operational amplifier as positive clipper and show output waveform. **(04)**

c) Draw circuit diagram of operational amplifier as adder where R_f=10kΩ, R_1=1kΩ, R_2=2kΩ V_1= 1 V, and V_2= -0.5V. Find output voltage. **(06)**

Q.2 **a)** What are the advantages of operational amplifier over transistor amplifier? State four specifications of operational amplifier. **(06)**

b) Draw block diagram of op amp and describe function of each block. What is the effect slew rate on output of op.amp? **(07)**

Q.3 **a)** Draw circuit diagram of op. amplifier as precision full wave rectifier and describe its operation with input and output waveforms. **(06)**

b) Draw diagram of Scmitt trigger and describe UTP and LTP with waveforms. **(07)**

Q.4 **a)** Describe working of operational amplifier as triangular wave generator with neat circuit diagram and waveforms **(06)**

b) Draw block diagram of IC 555 and describe its operation as table multivibrator **(07)**

SECTION – II

Q.5 **a)** Convert the following **(06)**
i) $(214)_8 = (\quad)_{10}$
ii) $(0.345)_{10} = (\quad)_8$
iii) $(110110001010)_2 = (\quad)_8$

b) With neat diagram explain the interfacing of TTL with CMOS IC **(04)**

c) With truth table and block diagram explain Half adder. **(04)**

Q.6 **a)** Design a 3 bit binary to gray code converter with neat block diagram and truth table. **(07)**

b) Evaluate the following with 2's complement method **(06)**
i) 110110-10110
ii) 10100.01-1011.10

Q.7 **a)** What is noise margin? Define it. Draw the logic signal voltage levels for TTL logic and indicate noise margin in it. **(07)**

b) Draw and explain working of two input TTL NAND gate working of totem pole output stage **(06)**

Q.8 **a)** Design the following logic expression using single 8:1 multiplexer. **(07)**
$F(a, b, c, d) = \sum m(0, 2, 3, 6, 8, 10, 14) + d(12, 13, 15)$

b) With neat block diagram explain BCD addition of two 4 bit numbers. **(06)**

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