B. TECH. (CBCS - 2014 COURSE) SEM - VIII (ELECTRONICS)
: SUMMER - 2018

SUBJECT : ELECTIVE – II : SYSTEM ON CHIP (SOC)

Day : **Saturday** **S-2018-4685** Time : **02.30 PM TO 05.30 PM**
Date : **09/06/2018** Max. Marks : 60

N. B. :

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Draw neat and labeled diagram **WHEREVER** necessary.
4) Assume suitable data, if necessary.

Q. 1 **a)** Draw and explain SOC design flow in brief. **(05)**

b) State the characteristics of typical deep submicron integrated circuit design. Explain the challenges faced by SOC design team. **(05)**

OR

Q. 1 Describe in brief: An improved design methodology for SOC design. **(10)**

Q. 2 Explain the software structure in SOC design. Also discuss software trends. **(10)**

OR

Q. 2 Describe the current SOC design flow. Explain important incremental tool enhancements. **(10)**

Q. 3 What are the essentials of SOC design methodology? Draw and explain: Advanced SOC design flow. **(10)**

OR

Q. 3 How the advanced SOC design helps in solving six key problems of existing SOC design? Discuss in brief. **(10)**

Q. 4 **a)** Write down the non processor building blocks in complex SOC **(05)**

b) Discuss the hardware interconnect mechanism with buses design. **(05)**

OR

Q. 4 Explain major decisions in processor-centric SOC organization. **(10)**

Q. 5 What are the different methods used for optimizing processor to match hardware? **(10)**

OR

Q. 5 Describe in detail: Pipelining for processor performance using simple RISC pipelines. **(10)**

Q. 6 Describe the following in detail: **(10)**

i) SOC and ROI
ii) The Designer's Dilemma

OR

Q. 6 What are the future applications of complex SOC? **(10)**

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