M. TECH.-I (ELECTRONICS V.L.S.I.) (CBCS – 2015 COURSE)

: SUMMER - 2018

SUBJECT: DIGITAL VLSI DESIGN

Day: **Wednesday** | **S-2018-2975** | Time: **11.00 AM TO 02.00 PM**

Date: **30/05/2018** | Max. Marks: 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in **SEPARATE** answer book.
4) Assume suitable data if necessary.
5) Use of non-programmable **CALCULATOR** is allowed.

SECTION – I

Q.1 Discuss following w.r.t. VHDL. **(10)**

a) Data Types

b) Data Flow Modeling

OR

Q.1 What are the objectives of VHDL? Explain the concept of entity in VHDL. **(10)**

Q.2 With suitable example, explain Generate statement. **(10)**

OR

Q.2 Design 8 – bit odd parity checker using structural modeling. Assume 2 – input XOR gate as a component. **(10)**

Q.3 Design BCD counter using FSM. **(10)**

OR

Q.3 Explain Assert and Report statements. **(10)**

SECTION - II

Q.4 Discuss Digital Design Flow. **(10)**

OR

Q.4 Explain Functional and Timing simulation in brief. **(10)**

Q.5 Compare FPGA and CPLD referring to architecture. **(10)**

OR

Q.5 Discuss various Modes of Configuration. **(10)**

Q.6 Design following using PLA: **(10)**

$f_0 = \sum m(0, 1, 4, 6)$

$f_1 = \sum m(2, 3, 4, 6, 7)$

$f_2 = \sum m(0, 1, 2, 6)$

OR

Q.6 With suitable example, discuss the implementation of 6 and 7 variable functions using FPGA. **(10)**

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