B. TECH. SEM - III (COMPUTER ENGG.) 2014 COURSE) (CBCS)
: SUMMER - 2018
SUBJECT; DIGITAL TECHNIQUES AND LOGIC DESIGN

Day: **Wednesday** | **S-2018-2237** | Time: **02.30 PM TO 05.30 PM**
Date: **23/05/2018** | Max Marks: 60

N.B.:

1) All questions are **COMPULSORY**.
2) Figures to the right indicate **FULL** marks.
3) Assume suitable data, if necessary.
4) Draw neat diagram **WHEREVER** necessary.

Q.1 Concert the following decimal numbers ints their equivalent binary, octal and hexadecimal numbers. **(10)**

i) 259 ii) 85.63 iii) 105

OR

a) Reduce the following expression and implement using NAND gates. **(05)**

$Y = A + \overline{A}B + AB$

b) Minimize the following expression using K-map **(05)**

$Y = \sum m(0,1,2,5,13,15)$

Q.2 Implement the following Boolean function using 4:1 multiplexers. **(10)**

$f(A,B,C,D,E,) = \sum m(0,1,2,3,6,8,9,10,13,15,17,20,24,)$

OR

Draw and explain four bit binary full adder How will you convert four bit binary adder to BCD adder? Explain with circuit diagram. **(10)**

Q.3 Draw neat diagram of J-K flip flop using S-R flip flop. Write truth table and explain race around condition. **(10)**

OR

Explain the working of four bit ripple counter using T flip flop. Draw circuit diagram and timing diagram. **(10)**

Q.4 Draw structure of EPROM. Explain how EPROM programming is carried out. **(10)**

OR

Describe operation of bipolar static RAM cell with neat diagram. **(10)**

Q.5 Compare CPLD and FPGA with the help of structural block diagram. **(10)**

OR

What is PLA? Draw combinational circuit for PLA with three inputs, three product terms and two outputs. **(10)**

Q.6 What is data flow model? Write the Architecture body for two input XOR gate using data flow model. **(10)**

OR

What is VHDL ? Write entity and Architecture declaration for two input AND and two input OR gate. **(10)**

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