B.TECH SEM - IV (2007 COURSE) (E & TC ENGG.) :
SUMMER - 2018
SUBJECT: DIGITAL ELECTRONICS

Day: **Thursday** Time: **10.00 AM TO 01.00 PM**
Date: **07/06/2018** Max Marks: 80

S-2018-2646

N.B. :

1) **Q.No.1** and **Q.No.5** are **COMPULSORY**. Out of remaining questions attempt **ANY TWO** questions from each section.
2) Answers to both the sections should be written in a **SEPARATE** answer books.
3) Figures to the right indicate **FULL** marks.
4) Assume suitable data, if necessary.

SECTION – I

Q.1 **a)** Explain current sourcing and current sinking in TTL logic family. **(05)**

b) Perform following operations using 2's complement method. **(04)**
i) 92 H – CD H **ii)** 89 D – 134 D
H- Hexadecimal
D- Decimal

c) With a neat diagram, explain the operation of PLA. **(05)**

Q.2 **a)** Draw and explain the operation of 2 input TTL open collector output NAND gate. **(07)**

b) Define following parameters with respect to logic families. **(06)**
i) Fan out **ii)** Power Dissipation **iii)** Propagation delay

Q.3 **a)** Design BCD code to Gray code converter and draw gate level diagram. **(06)**

b) Simplify following function using K-maps. **(07)**
$F(A,B,C,D)= \sum m(1,2,4,5,6,7,12,13,15)$

Q.4 **a)** Implement following function using 16:1 multiplexer. **(07)**
$F(a,b,c,d)= \sum m(2,4,5,7,10,11,14,15,18,21,25,26,30,31)$

b) Realize 64:1 multiplexer using 4:1 multiplexer. **(06)**

SECTION – II

Q.5 **a)** Explain the operation of 4-bit bidirectional shift register. **(05)**

b) Compare Mealy and Moore machine. **(04)**

c) What are the different types of memories? **(05)**

Q.6 **a)** Design a 3-bit binary up/ down ripple counter. **(07)**

b) Explain the operation of clocked SR- flip-flop with neat diagram. **(06)**

Q.7 **a)** Explain the operation of binary weighted DAC. **(06)**

b) Design a state machine to detect a sequence .....011.... **(07)**

Q.8 **a)** Compare SRAM and DRAM. **(07)**

b) Write a note on: **i)** NVRAM **ii)** EEPROM **(06)**

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