B.TECH SEM - III (2007 COURSE) (COMPUTER ENGG.) :
SUMMER - 2018
SUBJECT: DIGITAL LOGIC TECHNIQUES

Day : **Wednesday** **S-2018-2569** Time : **02.30 PM TO 05.30 PM**
Date : **23/05/2018** Max. Marks: 80

N. B. :

1) **Q. No.1 and Q. No.5 are COMPULSORY.** Out of remaining attempt **ANY TWO** questions from each section.
2) Figures to the right indicate **FULL** marks.
3) Answers to both the sections should be written in the **SEPARATE** answer book.
4) Neat diagrams must be drawn **WHEREVER** necessary.

SECTION-I

Q.1 **a)** Carry out following conversion: **(06)**
i) $(365.24)_8 = (\quad)_{10}$
ii) $(10110)_2 = (\quad)_{16}$
iii) $(86.63)_{10} = (\quad)_2$

b) Compare the performance of TTL, CMOS and ECL logic. **(04)**

c) Design conversion logic to convert JK flip flop into D flip flop. **(04)**

Q.2 **a)** Illustrate NAND and NOR are universal gales will the help of neat logic diagrams. **(07)**

b) Simplify following function using K maps. **(06)**
$Y = \Sigma m(1,5,6,7,11,12,13,15)$

Q.3 **a)** Describe operation of TTL tristate inverter with the help of neat circuit diagram. **(07)**

b) Design full subtractor using 1:8 demultiplexer. **(06)**

Q.4 **a)** Describe following flip flops with neat circuit diagrams and truth tables. **(07)**
i) Clocked SR ii) JK iii) D iv) T

b) Design and implement 3 bit up/down Asynchronous counter using JK FF **(06)**

SECTION-II

Q.5 **a)** Classify different types of ROM and state their applications. **(06)**

b) What is lockout condition? How it can be avoided ? **(04)**

c) What is PLD? Distinguish between PAL and PLA. **(04)**

Q.6 **a)** Describe the structure of Dynamic RAM cell? Explain why Refreshing is required in DRAM. **(07)**

b) Describe structure of TTL RAM cell. State its design parameter. **(06)**

Q.7 **a)** Design and draw 3 bit synch counter which goes through following states 1-3-5-7-1 **(07)**

b) Distinguish between Moore and Mealy model with the suitable examples. **(06)**

Q.8 **a)** Describe architecture of FPGA with neat diagram. How it is programmed. **(07)**

b) What is VHDL? Write Entity and Architecture declaration for 2 input AND gate and 2 input OR gate. **(06)**

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