B. TECH. SEM - III (ELECTRONICS) 2014 COURSE) (CBCS) :
SUMMER - 2018
SUBJECT: DIGITAL LOGIC CIRCUITS

Day: **Thursday** Time: **02.30 PM TO 05.30 PM**
Date: **24/05/2018** **S-2018-2247** Max Marks. 60

N.B.

1) All questions are **COMPULSORY.**
2) Figures to the right indicate **FULL** marks.
3) Assume suitable data , if necessary.
4) Draw neat diagram **WHEREVER** necessary.

Q.1 Minimize the following expressions using K – map and realize the same using basic gates. **(10)**

i)Y = $\sum$m (1,3,4,5,7,9,11,13,15)

ii) Y= $\sum$m(1,2,9,10,11,14,15)

OR

Q.1 Discuss the following reduction techniques with the help of advantages and disadvantages. **(10)**

i) Simplification using Boolean algebra laws

ii) Karnaugh map

iii) Quine Mccluskey method

Q.2 **a)** Design a parity generator using the basic gates to produce digital words with odd parity. Assume the input to be three bit binary words. **(06)**

b) Compare Encoder and decoder **(04)**

OR

Q.2 Design and implement a 2-bit comparator using suitable gates. **(10)**

Q.3 Describe the following three types of output configurations. **(10)**

i) Open Collector output

ii) Totem pole output

iii) Three state or tristate output

OR

Q.3 Describe the following term with respect to logic families & give their typical values for standard TTL, CMOS & ECL families. **(10)**

i) Fan-out ii) Propagation Delay

iii) Noise margin iv) figure of merit

Q.4 Write the state table, draw the state diagram and write the state equation for the following flip flops. **(10)**

i) Clocked D flip flop ii) Clocked JK FF

P.T.O

OR

Q.4 **a)** Describe the working of master slave JK flip–flop with the help of neat diagram. **(06)**

b) What is the function of preset and clear inputs in flip–flop? **(04)**

Q.5 **a)** Design a Modulo–5 ripple counter using a 3 bit ripple counter. **(06)**

b) Compare synchronous & Asynchronous counter. **(04)**

OR

Q.5 Design a sequence generator using JK flip flops **(10)**
1001001

Q.6 Compare the following : **(10)**
i) RAM & ROM
ii) SRAM & DRAM
iii) EPROM & EEPROM

OR

Q.6 Design and implement 3 – bit Binary to Gray code converter using PLA. **(10)**

* * *